



PATENT  
Docket No.: ACT-280COA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2185

Examiner: Not Yet Assigned

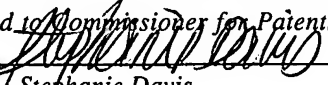
Serial No.: 10/722,636

Filed: November 25, 2003

In re Application of: Plants et al.

For: DELAY LOCKED LOOP FOR AN FPGA ARCHITECTURE

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 3/23/04. Signed  Stephanie Davis

TRANSMITTAL LETTER

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Enclosed please find the following:

1. Information Disclosure Statement;
2. Form PTO-1449
3. Copies of 19 References.

In the event any additional fee is required for filing the above-noted document, including any fees required under 37 CFR 1.136 for any necessary Extension of Time to make the filing of attached document timely, the Assistant Commissioner is hereby authorized to charge the fee to our Deposit Account No.: 50-0612.

Respectfully submitted,  
SIERRA PATENT GROUP, LTD.



Michael R. Johnson  
Reg. No.: 55,306

Dated: March 23, 2004

Sierra Patent Group, Ltd.  
P.O. Box 6149  
Stateline, NV 89449  
(775) 586-9500



PATENT

Docket No.: ACT-280COA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2185

Examiner: Not Yet Assigned

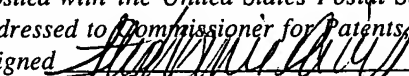
Serial No.: 10/722,636

Filed: November 25, 2003

In re Application of: Plants et al.

For: DELAY LOCKED LOOP FOR AN FPGA ARCHITECTURE

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 3/23/04. Signed 

Stephanie Davis

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Each item of information listed in the attached FORM PTO-1449, for which a copy of each is attached, may be material to the examination of the above-identified application and is, therefore, submitted in compliance with the duty of disclosure defined in 37 CFR §§1.56, 1.97 and 1.98. The Examiner is requested to make these items of official record in this application.

This Information Disclosure Statement under 37 CFR §§1.56, 1.97 and 1.98 is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that any one or more of these items constitutes prior art.

I

This statement is filed pursuant to:

( X ) 37 C.F.R. §1.97(b).

This information disclosure statement is filed either (1) within three months of the filing date of the national applications; (2) within three months of the date of entry of the national stage as set forth in 37 C.F.R. §1.491 in an international application; or (3) before the mailing date of a first office action on the merits, whichever event occurs last.

Accordingly, this information disclosure statement requires no fee and no certification.

( ) 37 C.F.R. §1.97(c).

This information disclosure statement is filed after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of either (1) a final action under 37 C.F.R. §1.113 or (2) a notice of allowance under 37 C.F.R. §1.311.

Accordingly, this information disclosure statement requires either the fee specified in 37 C.F.R. § 1.17 (p) or a statement according to 37 C.F.R. §1.97(e).

( ) 37 C.F.R. §1.97(d).

This information disclosure statement is filed after the period specified in 37 C.F.R. §1.97(c) and filed on or before the payment of the issue fee and is accompanied by

- (1) The statement specified in paragraph (e) of this section; and
- (2) The fee set forth in §1.17(p).

Accordingly, this information disclosure statement requires the fee specified in 37 C.F.R. §1.17(p), \$180.00, for submission of an information disclosure statement under 37 C.F.R. §1.97(d).

37 C.F.R. §1.97(e).

- ( ) (1) Each item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the statement.

- ( ) (2) No item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. §1.56(c), more than three months prior to the filing of the statement.

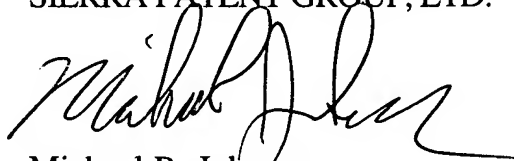
If this statement crosses in the mail with an office action, or is otherwise not in the indicated category of 37 C.F.R. §1.97, it is respectfully requested that this statement be treated in the next appropriate category and made of record. To the extent required, please treat this paper as a conditional petition for acceptance of the information disclosure statement.

II

- ( X ) No fee is due.
- ( ) The fee specified in 37 C.F.R. §1.17(p) for submission of an information disclosure statement under 37 C.F.R. §1.97(c) or 37 C.F.R § 1.97(d) is enclosed, \$180.00.

In the event any fee is required for filing the above-noted document, including any fees required under 37 CFR 1.136 for any necessary Extension of Time to make the filing attached document timely, the Assistant Commissioner is hereby authorized to charge the fee to our Deposit Account No. 50-0612. A duplicate of this page is enclosed.

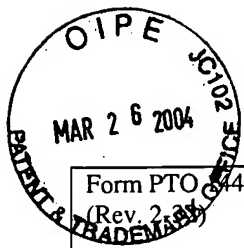
Respectfully submitted,  
SIERRA PATENT GROUP, LTD.



Michael R. Johnson  
Reg. No.: 55,306

Dated: March 23, 2004

Sierra Patent Group, Ltd.  
P.O. Box 6149  
Stateline, NV 89449  
(775) 586-9500  
(775) 586-9550 Fax



Form PTO 449 (Rev. 2-23-94) U.S. Department of Commerce Patent and Trademark Office				Atty. Docket No. ACT-280COA		Serial No. 10/722,636		
<b>Information Disclosure Statement by Applicant</b>				Applicant: Plants et al.				
(Use several sheets if necessary)				Filed: November 25, 2003 Group: 2185				
<b>U.S. Patent Documents</b>								
Init.		Document No.	Date	Name	Class	Subclass	Filing Date	
	1	5,666,322	09/09/1997	Conkle	365	233	09/21/1995	
	2	5,994,934	11/30/1999	Yoshimura et al.	327	158	07/08/1998	
	3	6,043,677	03/28/2000	Albu et al.	326	39	10/15/1997	
	4	6,111,448	08/29/2000	Shibayama	327	293	09/10/1998	
	5	6,181,174 B1	01/30/2001	Fujieda et al.	327	158	09/23/1999	
	6	6,289,068 B1	09/11/2001	Hassoun et al.	375	376	06/22/1998	
	7	6,292,016 B1	09/18/2001	Jefferson et al.	326	39	06/05/2000	
	8	6,437,650 B1	08/20/2002	Sung et al.	331	25	05/15/2001	
<b>Foreign Documents</b>								
Translation								
Init.		Document No.	Date	Country	Class	Subclass	Yes	No
	9	EP 1 137 188 A2	09/26/2001	Europe	H03L	07/08		X
	10	EP 1 137 188 A3	08/13/2003	Europe	H03L	07/08		X
<b>Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)</b>								
	11	L. Ashby, "ASIC Clock Distribution as a Phase Locked Loop (PLL)", <u>Proceedings Fourth Annual IEEE International ASIC Conference and Exhibit</u> , pp. 6.1-6.3, September 1991.						
	12	"AV9170 Application Note: Clock Synchronizer and Multiplier" AvaSem Corp, pp. 1-8, November 1992						
	13	AV9170 Application Note Preliminary Information, AvaSem, pp. 1-6, January 1993						
	14	U. Shannon et al., "A 30-ps JITTER, 3.6 us Locking, 3.3-Volt Digital PLL for CMOS Gate Arrays", IEEE 1993 Custom Integrated Circuits Conference, pp. 23.3.1-23.3.4, Conf. Date: May 9-12, 1993.						
	15	A. Efendovich et al., "Multi-Frequency Zero-Jitter Delay-Locked Loop", IEEE 1993 Custom Integrated Circuits Conference, pp. 27.1.1-27.1.4, Conf. Date: May 9-12, 1993.						
	16	R. Quinnell, "Blending gate arrays with dedicated circuits sweetens ASIC development", EDN, pp. 29-32, March 31, 1994.						
	17	J. Chen, "PLL-based clock systems span the system spectrum from green PCs to Alpha", EDN, pp. 147-155, November 9, 1995.						
	18	P. Sevalia, "Straightforward techniques cut jitter in PLL-based clock drives", EDN, pp. 119-125, November 23, 1995.						
	19	D. Bursky, "Memories Hit New Highs And Clocks Run Jitter-Free", Electronic Design, pp. 79-93, February 19, 1996.						
Examiner					Date Considered			
Examiner: Initial if citation considered, whether or not citation is in conference with MPEP 609; Draw line through citation if not conformance and not considered. Include a copy of this form with the next communication to applicant.								